Serial Data Hub

Project Plan

Senior Design Group DEC13-13
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Client: Dr. Koray Celik

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Introduction and Problem Statement:

Members of an Iowa State research team are developing autonomous robots to map floor plans of an unknown building. For any robotics development, debugging requires sending and gathering data with a component. There exist many one-to-one signal conversion products; however, they would each run independent of each other and would destabilize the synchronization of data. For assistance in their robotics development, they require a tool to serially communicate with multiple components of the robot at once. For this, Dr. Koray Celik, has requested that we build a serial data hub to connect a laptop to sixteen different serial devices.

Objective and System Description:

Our objective is to build a serial data hub. The peripheral will be a separate module that connects to a Linux laptop by a USB cable and then connects to sixteen other serial ports on various robotics components of a machine. The hardware logic will be implemented on an Altera Cyclone II FPGA mounted on a PCB board with RS-232 connectors. The FPGA will run firmware with Altera's Nios II soft-core processor. Communication will be handled via an API on a laptop running Ubuntu v11.04.

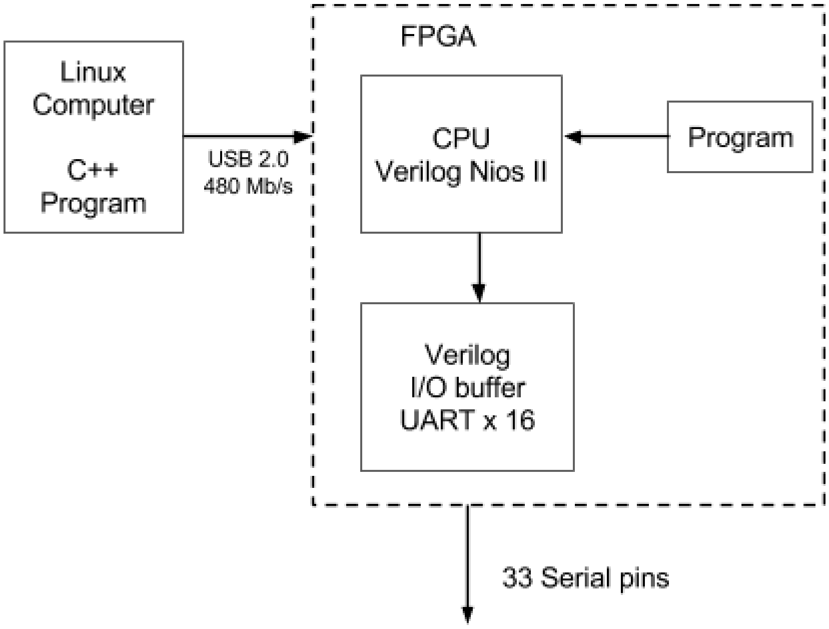
Functional Requirements:

- System must provide multiple serial port interfaces to connect robotics peripheral components
- System must provide a serial port interface to connect to controlling PC
- System must transfer data between PC and component in a way that ensures no data is lost (guarantees data integrity)
- System must manage 16 to 1 data throughput channels
- System must transfer data in a prompt manner to reflect real-time systems
- System must be controlled by an API library on the PC

Non Functional Requirements:

- System shall implement an Altera Nios II soft processor.
- System shall use the soft processor to run firmware code on FPGA.
- System shall be prototyped on Altera's DE2 Development Board
- System shall use USB 2.0 to communicate between the FPGA and the PC API.
- System shall use same USB controller as the DE2 Board
- System shall have 16 serial ports implementing RS-232 on DB9 connectors
- System shall use external memory modules rather than FPGA memory

System Block Diagram:



Assumptions/Design Choices/Operation Conditions:

-Will be running an Altera Nios II soft processor on an Altera Cyclone II FPGA
-Will be using no parity check on UART
-Will assume serial components follow UART capabilities
-Will be using memory hardware external to the FPGA
-Will be using the USB controller akin to the one on the DE2 board
-End product will be needed in an end application for ground robots.
-API support is guaranteed for, but not limited to, Ubuntu 11.04. Drivers may or may not work on other operating systems.
-Will be using Altera's DE2 development board for prototyping.

Material List:

Below is a list of hardware and software materials and tools that will be used for the project.

Hardware:

-Altera Cyclone II FPGA development board (DE2)
-Laptop with Linux Ubuntu v11.04

Software:

-Altera Quartus II:

A licensed Altera software tool used for analysis and synthesis of hardware descriptive language (HDL) design. This program enables the developer to compile their design, perform timing analysis, simulate designs and configure the target device.

-ModelSim:

A licensed software tool that help simulates, compiles, and debugs VHDL or Verilog designs without loading the design on a FPGA.

-MegaCore Library:

A licensed library for the Altera Quartus II software. This library contains a list of likened Altera cores. The Nios II embedded soft processor is located in this library.

Justification for Materials:

We decided to use an FPGA so that we could have access to a large number of programmable GPIO pins to support a large number of ports. The group decided to use an Altera Cyclone II DE2 development board which includes many useful hardware components already on it and it was a platform our group had familiarity with. Instead of programming hardware logic into the FPGA or using a pre-made processor, the group decided to use an Altera Nios II soft processor on our FPGA for easier modification at a later date

Researched Options:

There were two main options to approach this project. We could use a microcontroller and add supporting UART chips, and USB controller. The second option is that we could use an FPGA/development board and design hardware logic and firmware.

We chose to not use a microcontroller due to the lack of included UART modules and the lack of general IO pins available. Additionally we would not be able to guarantee synchronized buffering between the separate UART modules.

Below is the breakdown of research of each option.

1. Microcontroller with supporting chips

Items:	**Descriptions/Features:**	**Cost:**
Arduino Mega 2560	● ATmega2560 microcontroller (256 KB flash memory) ● 54 digital input/output pins (16 analog, 15 with PWM) ● 4 UARTs (hardware serial ports) ● clock speed 16 MHz ● USB connection	$55.56
Atmel Microprocessor: AT91SAM7S512	● Flash (Kbytes):512 Kbytes ● Pin Count:64 ● Max. Operating Freq. (MHz):55 MHz ● CPU: ARM7TDMI ● Max I/O Pins:32 ● USB Transceiver:1 ● USB Speed: Full Speed ● USB Interface: Device	$16.54
UART Chips: Texas Instrument: PC16550D	● FIFO mode transmitter and receiver are each buffered with 16 byte ● Fully programmable serial-interface characteristics: ○ 5-, 6-, 7-, or 8-bit characters ○ Even, odd, or no-parity bit generation and detection ○ 1-, 1½-, or 2-stop bit generation ○ Baud generation (DC to 1.5M baud). ● False start bit detection.	16 x $7.55 =$120.80
USB Controller: Philips ISP1362	● Data transfer at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) ● Controllable LazyClock (110 kHz ± 50 %) output during ‘suspend’ ● Operates at 3.3 V power supply ● 12 MHz crystal or direct clock source with on-chip Phase-Locked Loop (PLL) ● 16-bit data bus ● 10 Mbyte/s data transfer rate between the microprocessor and ISP1362	$6.45

2. FPGAs/Development Boards

Items:	Descriptions/Features:	Cost:
Xilinx Zynq-7000 All Programmable SoC ZC702 Evaluation Kit	● 16MB Quad SPI Flash ● DDR3 Component Memory 1GB ● Support 32 data width ● USB OTG 1 (PS) - Host USB ● USB UART (PS) ● 12V wall adapter or ATX ● 33.33MHz Fixed PS System Oscillator (Single-Ended CMOS) ● FMC #1-LPC connector (0 GTX Transceiver, 68 single-ended or 34 differential user defined signals) ● FMC #2-LPC connector (0 GTX Transceiver, 68 single-ended or 34 differential user defined signals)	$895
Altera Cyclone II DE2 **(chosen option)**	**● Built-in USB-Blaster for FPGA configuration** **● USB 2.0 (type A and type B)** **● Expansion headers (two 40-pin headers)** **● Memory: 8 MB SDRAM, 512 KB SRAM, 4 MB Flash** **● Clock options: 50 MHz clock or 27 MHz**	**$269**

Deliverables:

- Either a PCB or a DE2 board containing an Altera Cyclone II FPGA loaded with a custom Nios II processor and firmware.
- Quartus project files for custom Nios II processor
- Verilog code for custom hardware module
- Firmware code to run on the soft processor
- Interconnect Schematics and System Block Diagrams
- Device Driver and API for Ubuntu 11.04 Linux Laptop

Constraints:

Time - The project must be completed by the end of the Fall 2013 semester.

Budget - While no specific amount has been set in stone, we are expected to limit our expenditures as much as possible. Many of the materials needed have been supplied by the client, including a DE2 board.

Risks/Challenges:

Below is a list of potential risks and solutions that may occur during the life cycle of the project.

Potential Risks	**Solutions**
If the group loses a member, how will tasks be redistributed?	Each team member was given a responsibility for each of their components. If for any reason one member leaves, that person’s task will be given to the team member with the most experience in the area of the task and/or the team member with the lesser amount of tasks.
If no access to software licenses?	First contact CSG or Jason Boyd (ISU Altera Contact) if a license could be obtained. Then contact the company responsible (Altera, SLS, etc) to see if a license could be provided. Third option is looking into Open Core software/design, or opinion of advisor and/or client.
If hardware fails/broken?	If there is a hardware issue, first verify it is not a software problem by testing with other DE2 boards (either in lab 2051 or borrow a board from the parts shop). If indeed a hardware problem, contact advisor to see if a part could be replace or contact Jason Boyd to see if an extra DE2 board could be borrowed until another DE2 board can be purchase.
If an unexpected bug/error occurs during integration?	Identify the component the bug/error is related to, then replicate the error and debug/test the individual component. Most likely the team member most familiar with the component would lead or assist the debugging process.
If a problem occurs for final demo?	Have a back-up board/demo ready. Maybe have a video recording of a working demo that could be displayed on a laptop.
If there is a code and documentation version control problem?	As a team we will have all our code and documentation on Google Drive, as well as Subversion or GIT. We will provide access of version control depositary as part of deliverables.

Initial Estimate of Timeline/Work Breakdown

Below is a list of tasks and estimated time, description, and task owner.

Task	Description	Time Estimate	Task Owner
UART Clk Divider	Design clock divider to go inside the UART receiver in Verilog. Design and run testbenches in simulation.	1 week	Darin and Adriana
UART Shifter	Design bit shifter to go inside the UART receiver in Verilog. Design and run testbenches in simulation.	1 week	Darin and Adriana
UART FIFO	Design the FIFO module for the UART receiver. Design and run testbenches in simulation.	1 week	Darin and Adriana
UART RX module	Combine clock divider, bit shifter, and FIFO with miscellaneous control logic to create the receiver module for the UART. Design and run testbenches in simulation.	1 week	Darin and Adriana
UART TX module	Copy the receiver module and then modify the direction of some bit streams to create the UART transmitter. Design and run testbenches for simulation.	1 week	Darin and Adriana
UART Monkey Testing	Detailed Testing of UART	2 weeks	Darin
Get API Req	Need to contact Koray to get specific API requirements for the C modules	1 week	Justin
Write Header Files	Write header files for API. Determine function return values and function parameters.	1 week	Justin
Write Simple USB Test Program	Based on initial research, USB supports a command that will identify a device connected to one of its ports. Write a test program that does just this.	2 weeks	Justin
Upload basic Nios II processor	Upload a simple version of the Nios II processor to one of the Altera Cyclone FPGA's. Write a simple C program for the processor. Upload and run the program off of the FPGA.	2 weeks	Steven

Store data from 17 locations into 2 buffers	Design the logic channels for communication between the 16 + 1 ports and the buffers for holding data	1 week	Steven
Firmware Interrupts	Implement an interrupt system for Firmware to send back to USB	2 weeks	Steven and Adriana
External Memory Modules	Develop interface to external memory modules with the Nios II processor or the firmware	3 weeks	Steven and Adriana
Interface with USB controller	DE2 board has an interface chip that controls the USB ports whether the FPGA is acting as a host or peripheral	2 weeks	Steven and Justin
Interface with UART module	Need to connect UART module to the Nios II processor.	1 week	Adriana and Steven
CRC Error Correction	Implement Error Correction System	1 week	Steven and Justin

Cost Breakdown

There are two paths our group can take in order to produce the final product. Option one is to design keeps the design on the DE2 board, and option two is to place the final design on a PCB.

DE2 Final Product Option	**Cost**	**PCB Final Project Option**	**Cost**
DE2 board	$269	PCB (5 units)	~$150
GPIO Connectors	~$7.95	Cyclone II FPGA	$150
D89 Connectors (8 units)	~$40	Max232 (16 units)	~$5
		Voltage Regulator	$70
Total Cost:	***~$316.95**	**Total Cost:**	**~$375**

*note: DE2 option is effectively only ~$47.95, since the client already has a spare DE2 board to be used.